

# DATA SHEET

## **74HC74; 74HCT74**

Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification  
Supersedes data of 1998 Feb 23

2003 Jul 10

## Dual D-type flip-flop with set and reset; positive-edge trigger

## 74HC74; 74HCT74

### FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

### GENERAL DESCRIPTION

The 74HC/HCT74 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nCP to nQ, n $\overline{Q}$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	14	15	ns
	n $\overline{SD}$ to nQ, n $\overline{Q}$		15	18	ns
	n $\overline{RD}$ to nQ, n $\overline{Q}$		16	18	ns
$f_{max}$	maximum clock frequency		76	59	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. For 74HC74 the condition is  $V_I = \text{GND to } V_{CC}$ .

For 74HCT74 the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ .

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## FUNCTION TABLES

Table 1 See note 1

INPUT				OUTPUT	
$\bar{S}D$	$\bar{R}D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2 See note 1

INPUT				OUTPUT	
$\bar{S}D$	$\bar{R}D$	CP	D	Q <sub>n+1</sub>	$\bar{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

## Note

- H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
↑ = LOW-to-HIGH CP transition;  
Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition.

## ORDERING INFORMATION

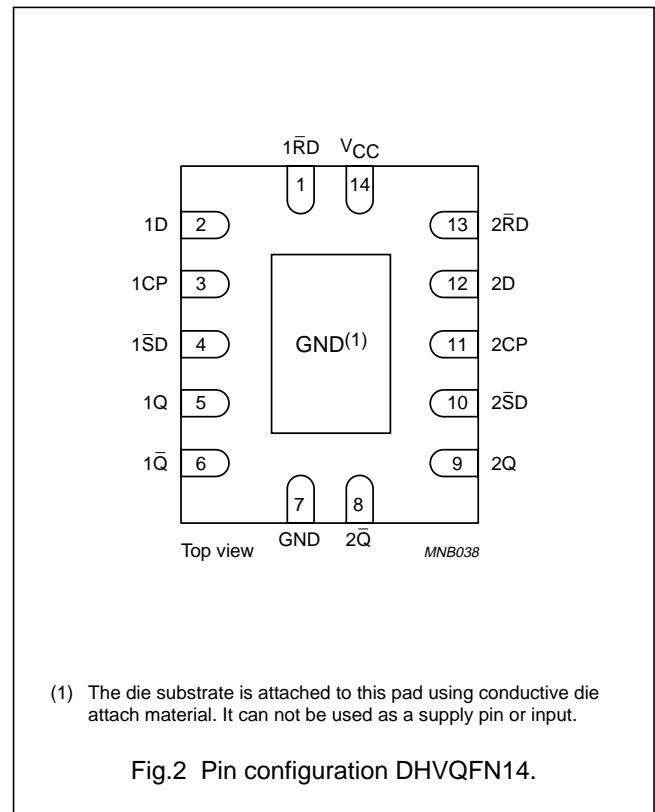
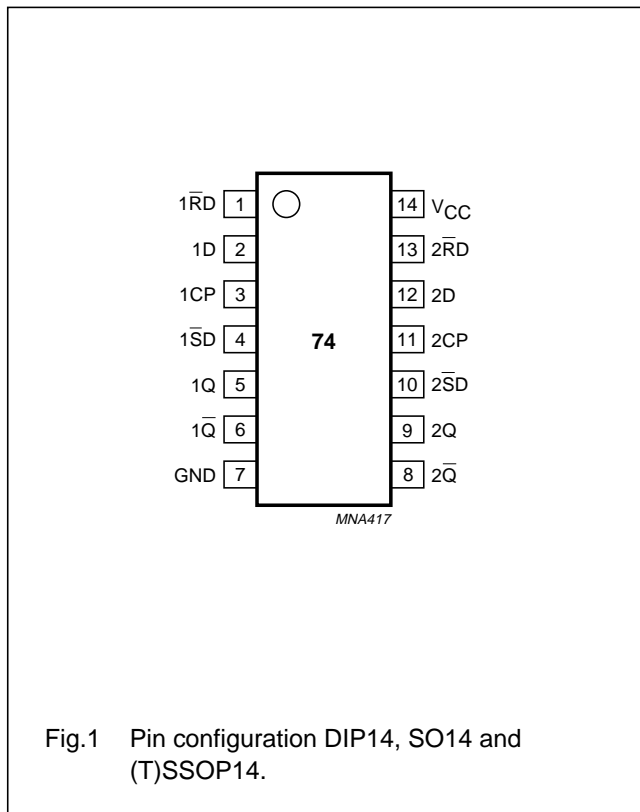
TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC74N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT74N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC74D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT74D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HC74DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT74DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC74PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT74PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC74BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT74BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

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## PINNING

PIN	SYMBOL	DESCRIPTION
1	1 $\overline{\text{RD}}$	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	1 $\overline{\text{SD}}$	asynchronous set-direct input (active LOW)
5	1Q	true flip-flop output
6	1 $\overline{\text{Q}}$	complement flip-flop output
7	GND	ground (0 V)
8	2 $\overline{\text{Q}}$	complement flip-flop output
9	2Q	true flip-flop output
10	2 $\overline{\text{SD}}$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	2 $\overline{\text{RD}}$	asynchronous reset-direct input (active LOW)
14	V <sub>CC</sub>	positive supply voltage



Dual D-type flip-flop with set and reset;  
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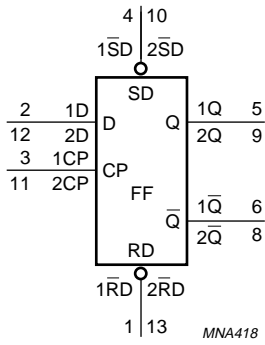


Fig.3 Logic symbol.

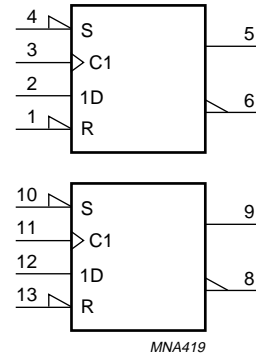


Fig.4 IEC logic symbol.

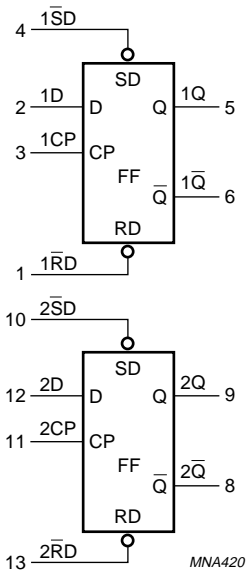


Fig.5 Functional diagram.

Dual D-type flip-flop with set and reset;  
positive-edge trigger

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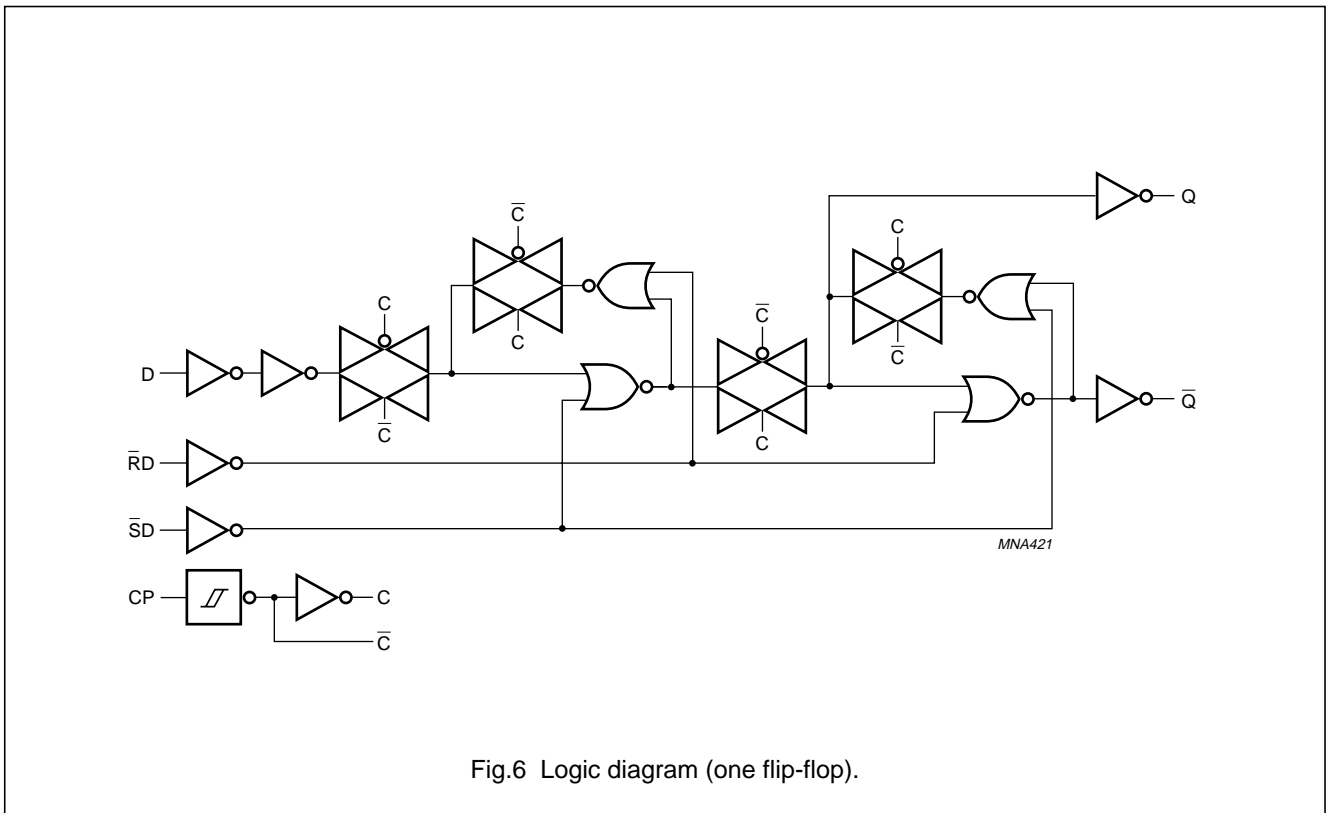


Fig.6 Logic diagram (one flip-flop).

Dual D-type flip-flop with set and reset;  
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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC74			74HCT74			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature		–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	500	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	500	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ ; note 1	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ ; note 1	–	±20	mA
$I_O$	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ ; note 1	–	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		–	±100	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ to }+125\text{ °C}$ ; note 2	–	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.  
For DIP14 packages: above 70 °C derate linearly with 12 mW/K.

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## DC CHARACTERISTICS

## Family 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -4.0 mA	4.5	3.84	4.32	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.34	5.81	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.33	V
		I <sub>O</sub> = 5.2 mA	6.0	–	0.16	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	40	μA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.2	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		I <sub>O</sub> = 5.2 mA	6.0	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	80	μA

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.



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## Family 74HCT

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4.0 mA	4.5	3.84	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4.0 mA	4.5	0.33	0.15	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input	V <sub>I</sub> = V <sub>CC</sub> -2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	4.5 to 5.5	–	100	450	μA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	80	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input	V <sub>I</sub> = V <sub>CC</sub> -2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	4.5 to 5.5	–	–	490	μA

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

## Remark to HCT types

The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table.

INPUT	UNIT LOAD COEFFICIENT
nD	0.70
nRD	0.70
nSD	0.80
nCP	0.80

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## AC CHARACTERISTICS

## Family 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄	see Fig.7	2.0	–	47	220	ns
			4.5	–	17	44	ns
			6.0	–	14	37	ns
	propagation delay nSD to nQ, nQ̄	see Fig.8	2.0	–	50	250	ns
			4.5	–	18	50	ns
			6.0	–	14	43	ns
	propagation delay nRD to nQ, nQ̄	see Fig.8	2.0	–	52	250	ns
			4.5	–	19	50	ns
			6.0	–	15	43	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Fig.7	2.0	–	19	95	ns
			4.5	–	7	19	ns
			6.0	–	6	16	ns
t <sub>w</sub>	clock pulse width HIGH or LOW	see Fig.7	2.0	100	19	–	ns
			4.5	20	7	–	ns
			6.0	17	6	–	ns
	set or reset pulse width LOW	see Fig.8	2.0	100	19	–	ns
			4.5	20	7	–	ns
			6.0	17	6	–	ns
t <sub>rem</sub>	removal time set or reset	see Fig.8	2.0	40	3	–	ns
			4.5	8	1	–	ns
			6.0	7	1	–	ns
t <sub>su</sub>	set-up time nD to nCP	see Fig.7	2.0	75	6	–	ns
			4.5	15	2	–	ns
			6.0	13	2	–	ns
t <sub>h</sub>	hold time nCP to nD	see Fig.7	2.0	3	–6	–	ns
			4.5	3	–2	–	ns
			6.0	3	–2	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Fig.7	2.0	4.8	23	–	MHz
			4.5	24	69	–	MHz
			6.0	28	82	–	MHz

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄	see Fig.7	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
	propagation delay nSD to nQ, nQ̄	see Fig.8	2.0	–	–	300	ns
			4.5	–	–	60	ns
			6.0	–	–	51	ns
	propagation delay nRD to nQ, nQ̄	see Fig.8	2.0	–	–	300	ns
			4.5	–	–	60	ns
			6.0	–	–	51	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Fig.7	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns
t <sub>w</sub>	clock pulse width HIGH or LOW	see Fig.7	2.0	120	–	–	ns
			4.5	24	–	–	ns
			6.0	20	–	–	ns
t <sub>w</sub>	set or reset pulse width LOW	see Fig.8	2.0	120	–	–	ns
			4.5	24	–	–	ns
			6.0	20	–	–	ns
t <sub>rem</sub>	removal time set or reset	see Fig.8	2.0	45	–	–	ns
			4.5	9	–	–	ns
			6.0	8	–	–	ns
t <sub>su</sub>	set-up time nD to nCP	see Fig.7	2.0	90	–	–	ns
			4.5	18	–	–	ns
			6.0	15	–	–	ns
t <sub>h</sub>	hold time nCP to nD	see Fig.7	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Fig.7	2.0	4.0	–	–	MHz
			4.5	20	–	–	MHz
			6.0	24	–	–	MHz

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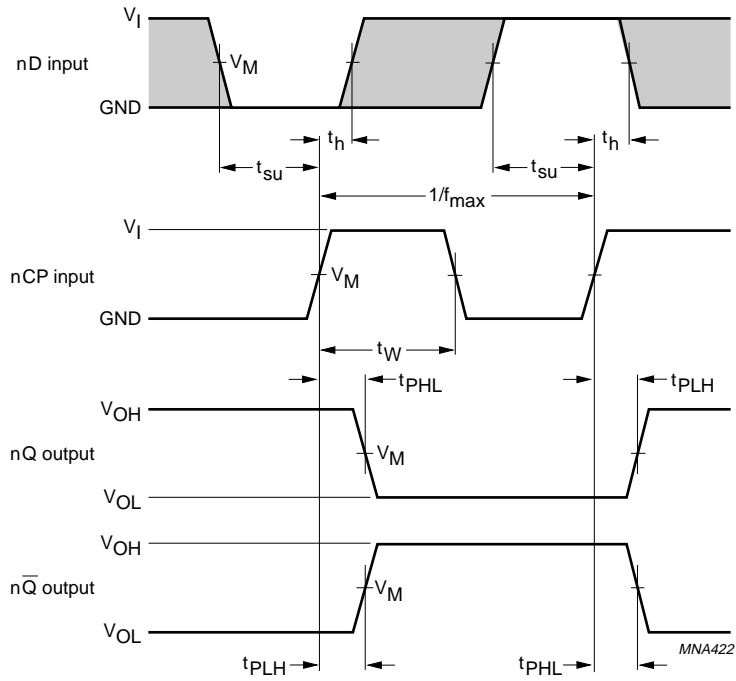
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nCP to nQ, n $\bar{Q}$	see Fig.7	4.5	–	18	44	ns
	propagation delay n $\bar{SD}$ to nQ, n $\bar{Q}$	see Fig.8	4.5	–	23	50	ns
	propagation delay n $\bar{RD}$ to nQ, n $\bar{Q}$	see Fig.8	4.5	–	24	50	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Fig.7	4.5	–	7	19	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see Fig.7	4.5	23	9	–	ns
	set or reset pulse width LOW	see Fig.8	4.5	20	9	–	ns
t <sub>rem</sub>	removal time set or reset	see Fig.8	4.5	8	1	–	ns
t <sub>su</sub>	set-up time nD to nCP	see Fig.7	4.5	15	5	–	ns
t <sub>h</sub>	hold time nCP to nD	see Fig.7	4.5	+3	–3	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Fig.7	4.5	22	54	–	MHz
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nCP to nQ, n $\bar{Q}$	see Fig.7	4.5	–	–	53	ns
	propagation delay n $\bar{SD}$ to nQ, n $\bar{Q}$	see Fig.8	4.5	–	–	60	ns
	propagation delay n $\bar{RD}$ to nQ, n $\bar{Q}$	see Fig.8	4.5	–	–	60	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Fig.7	4.5	–	–	22	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see Fig.7	4.5	27	–	–	ns
	set or reset pulse width LOW	see Fig.8	4.5	24	–	–	ns
t <sub>rem</sub>	removal time set or reset	see Fig.8	4.5	9	–	–	ns
t <sub>su</sub>	set-up time nD to nCP	see Fig.7	4.5	18	–	–	ns
t <sub>h</sub>	hold time nCP to nD	see Fig.7	4.5	3	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Fig.7	4.5	18	–	–	MHz

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74HC74; 74HCT74

## AC WAVEFORMS

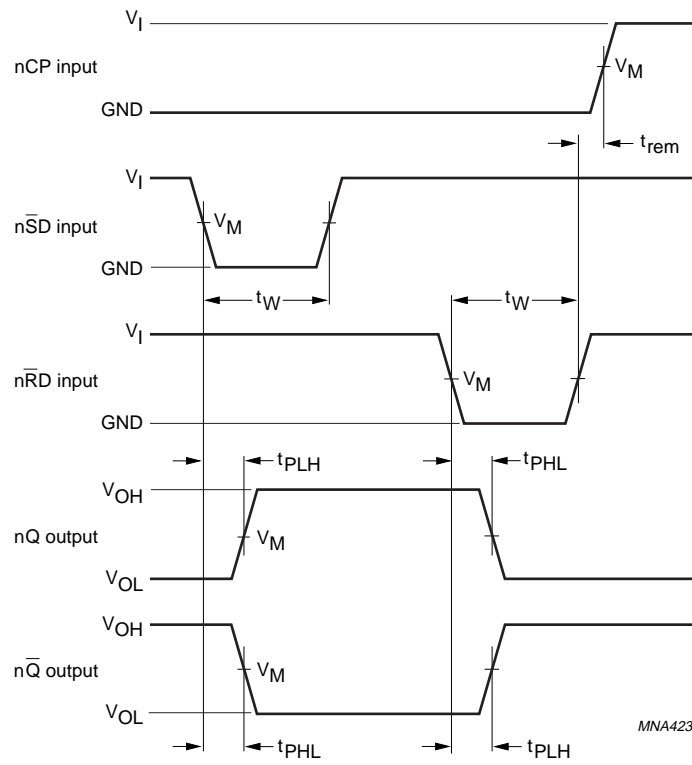


The shaded areas indicate when the input is permitted to change for predictable output performance.  
74HC74:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
74HCT74:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 The clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74

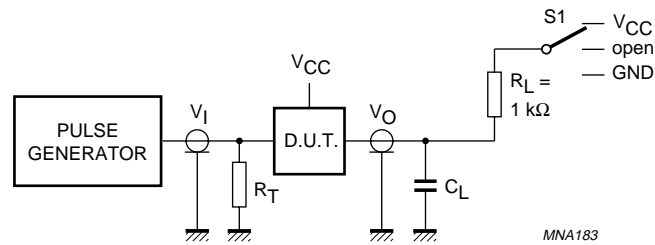


74HC74:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
74HCT74:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 The set ( $\overline{nSD}$ ) and reset ( $\overline{nRD}$ ) input to output ( $nQ$ ,  $\overline{nQ}$ ) propagation delays, the set and reset pulse widths and the  $\overline{nRD}$ ,  $\overline{nRD}$  to  $nCP$  removal time.

Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74



TEST	S1
$t_{pZH}$	GND
$t_{pZL}$	$V_{CC}$
$t_{pHZ}$	GND
$t_{pLZ}$	$V_{CC}$

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.9 Load circuitry for switching times.

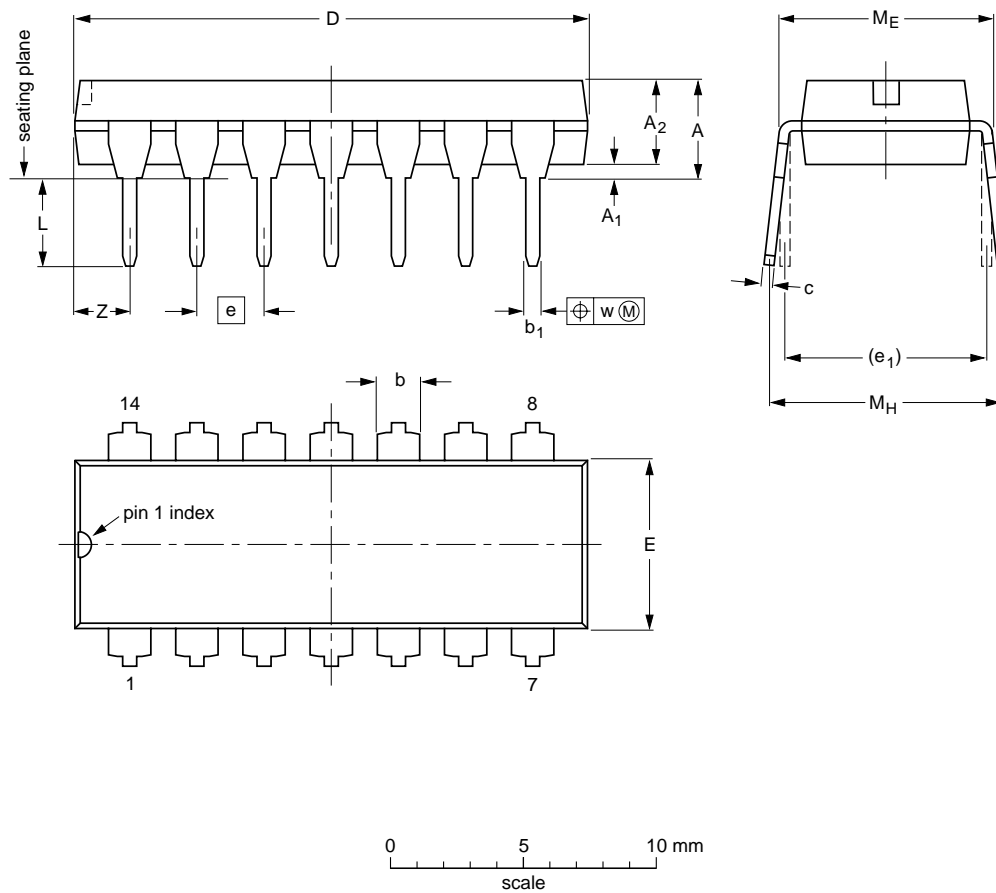
Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			99-12-27 03-02-13

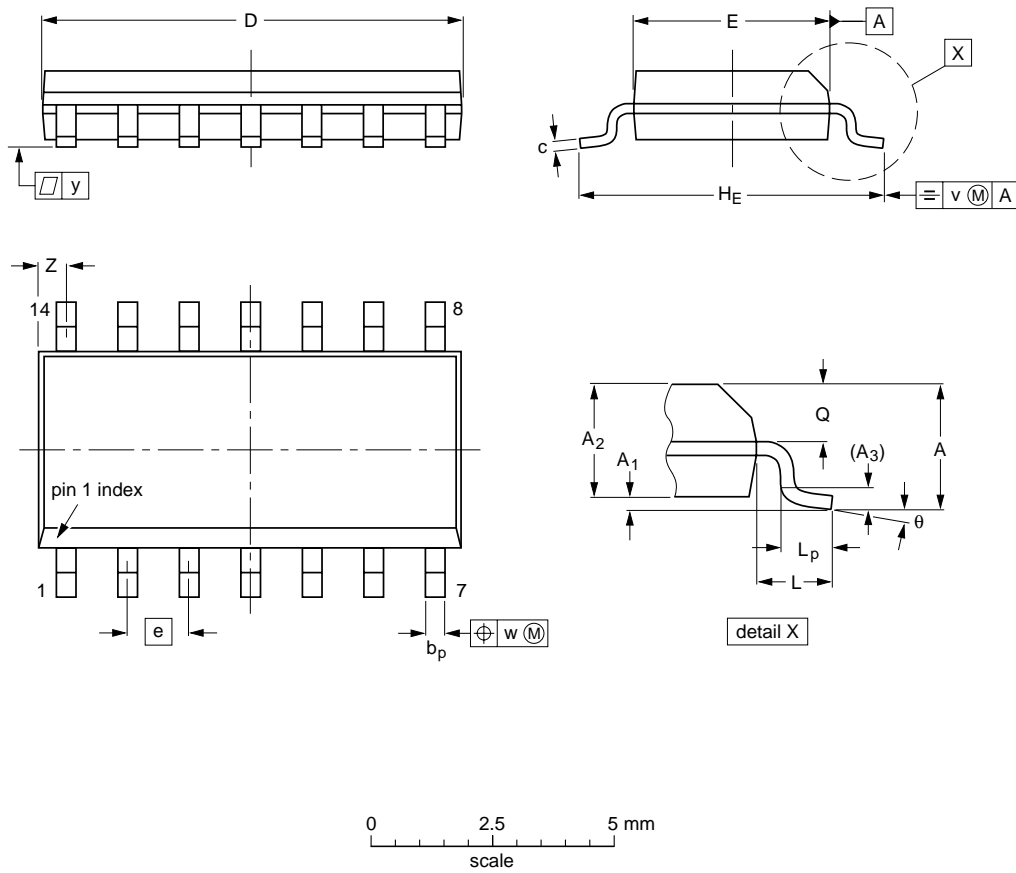


Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

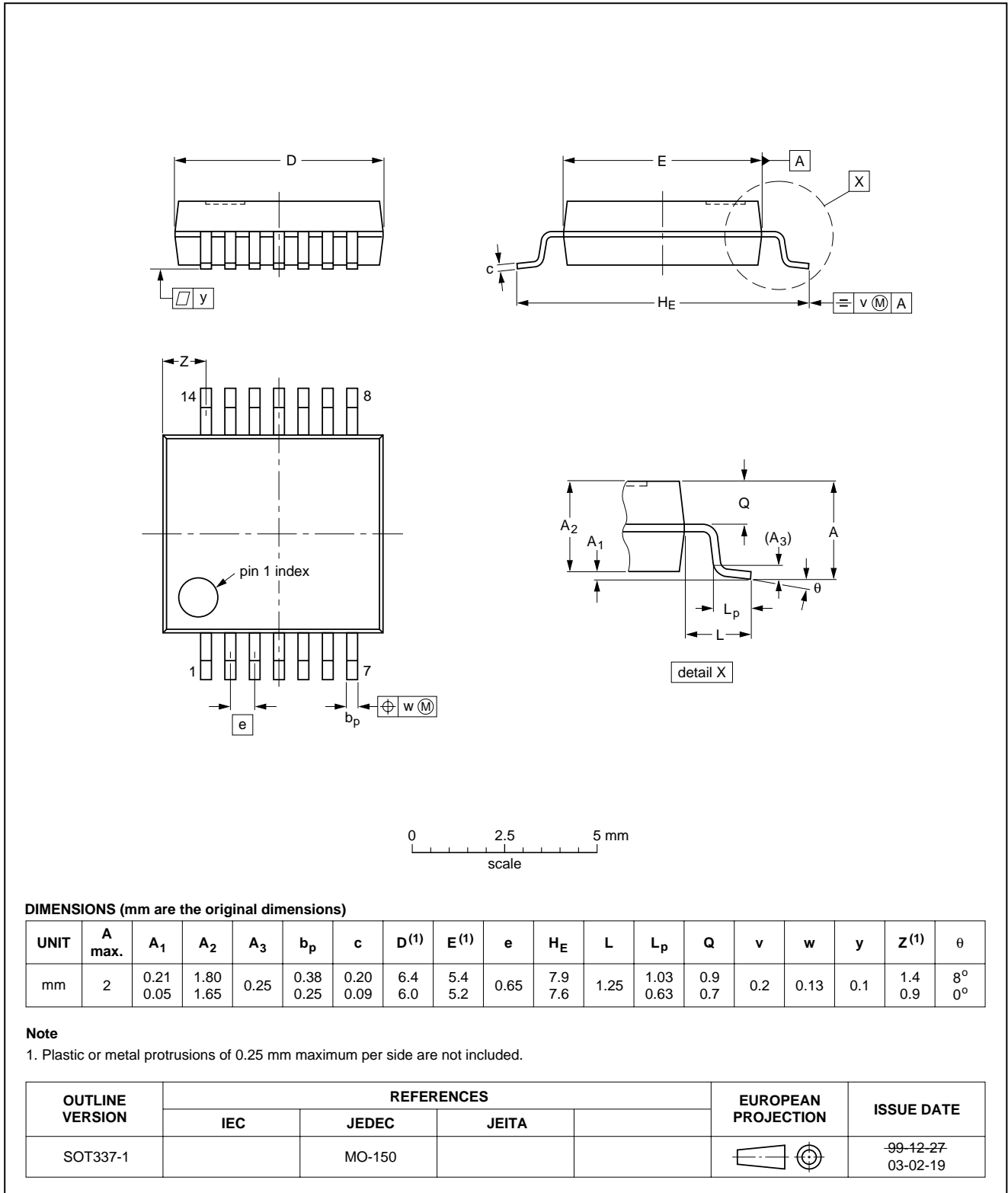
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

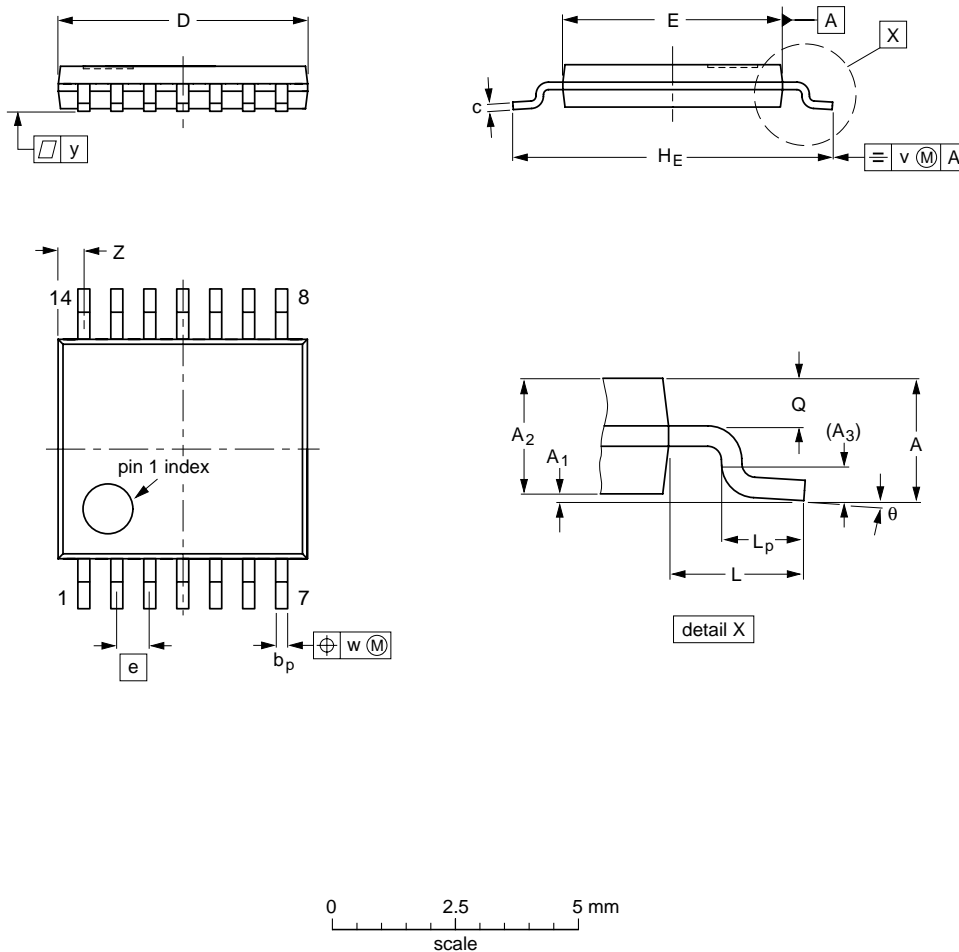


Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

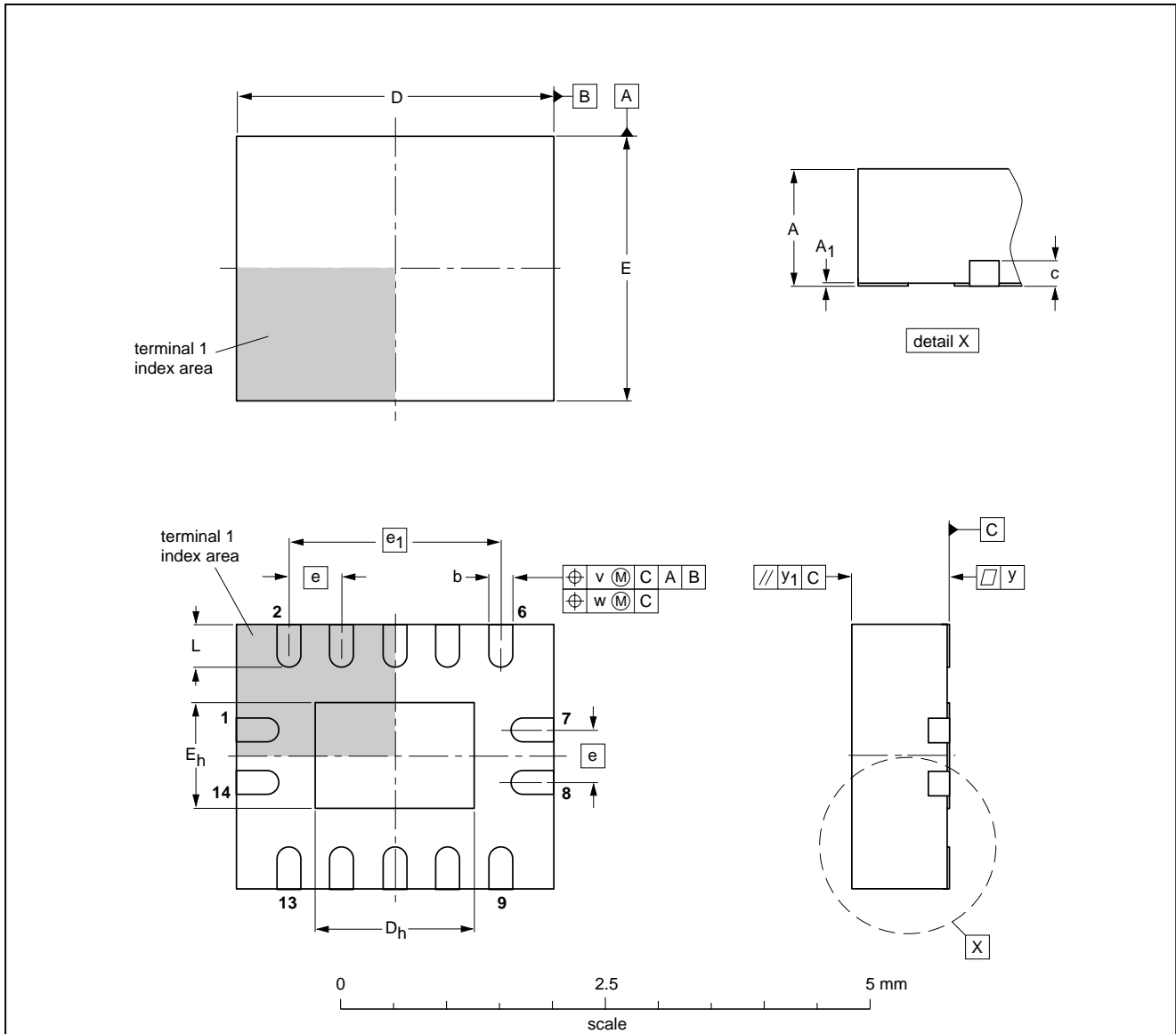
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Dual D-type flip-flop with set and reset;  
positive-edge trigger

74HC74; 74HCT74

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

## Dual D-type flip-flop with set and reset; positive-edge trigger

74HC74; 74HCT74

### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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